## REMARKS

Claims 1-12 and 18-23 are pending in the present application. As a result of a previous restriction requirement, claims 13-17 were cancelled. Claims 20-23 were allowed in the Office Action dated February 1, 2005. Claims 1, 8 and 18 are amended. Reconsideration of all rejected claims is respectfully requested in light of the amendments made and the arguments presented below.

**Claim Rejections under 35 USC 102**

Claims 1, 6-7 and 18-19 were rejected under 35 USC 102 as being anticipated by Chiu (US Patent No. 6,562,682).

Claim 1 is amended to include the limitation, "subsequently removing the sidewall elements thereby exposing surfaces of the first and second floating gate portions." No such limitation appears to be shown by Chiu. Spacers 210a of Chiu, identified as corresponding to sidewall elements, do not appear to be removed (Figure 2E). Because these elements are kept in place, the surfaces of the first and second floating gate portions remain unexposed. Therefore, it is submitted that the rejection is overcome.

The limitation added to claim 1 was previously recited in claim 8, which was rejected under 35 USC 103(a) as unpatentable over Chiu in view of Chuang (US Pub. No. 2004/0033663). However, this would not appear to form a basis for a rejection of claim 1 as amended because all claim elements are not shown by the combination and because no adequate motivation to combine the references has been shown.

Chuang was cited as showing the limitation "subsequently removing the sidewall elements thereby exposing surfaces of the first and second floating gate portions." However, the spacers 208a of Chuang appear to remain in place. Figure 2i of Chuang appears to show the final structure and clearly shows spacers 208a. While Figure 2h does not appear to show spacers 208a, there is no indication that they are removed and it appears that they are not removed because they are shown in the following drawing, Figure 2i. There also appears to be no disclosure of removing spacers 208a in the related text. Chiu does not appear to show this feature either. Because this feature is not shown

in either of the cited references, it is believed that claim 1 is allowable over these references.

Even if removal of spacers were shown by Chuang, there appears to be no adequate motivation to combine such a teaching with Chiu to obtain the combination of claim 1. "The prior art must suggest the desirability of the claimed invention," MPEP 2143.01. No indication of the desirability of removing sidewall elements is shown. The motivation cited in the rejection of claim 8 was "because the structure of Chiu et al. requires dielectric material formed over the floating gate portion for insulation." However, this does not address removal of sidewall elements. Chuang does not appear to provide any motivation for removing sidewall elements because this feature does not appear to be discussed. Chiu appears to teach away from such a modification because Chiu teaches a structure in which spacers 210a are covered over by a second conductive layer 214 which later forms parts of floating gates. Removing spacers 210a prior to deposition of conductive layer 214 would appear to negate an advantage of Chiu, "because of the protection of the oxide spacer 210a, the misalignment window for defining the second conductive layer is greatly increased," column 3, lines 56-59. Removing spacers 210a after deposition of conductive layer 214 would appear to require removal of at least a significant portion of layer 214 and it is not clear how this would be achieved. MPEP 2143.01 states, "The proposed modification cannot change the principle of operation of a reference." It is not seen how spacer 210a could be removed without changing the principle of operation of Chiu. Thus, Chiu appears to teach away from removal of spacers 210a and it would seem that any modification of the process of Chiu to remove these spacers would be contrary to the purpose stated by Chiu. "Since the oxide spacer (or the remained oxide layer) protects a portion of the underlying conductive layer, the misalignment window for defining the gate can be enlarged," column 1, lines 56-59.

Thus, claim 1 is submitted to be allowable because an additional limitation is added that overcomes the 35 USC 102 rejection over Chiu. Claim 1 as amended also appears to be allowable over a combination of Chiu and Chuang because the added limitation is not shown by either reference and modifying Chiu to include the limitation appears contrary to the teaching of Chiu.

Claims 2-12 depend from claim 1 and are submitted to be allowable at least as depending from an allowable base claim. In addition, claim 6 recites "the sidewall portions are formed by deposition and etch back of silicon nitride." Features 210 of Figures 2B-2C were cited as showing this feature. However, Chiu states, "the oxide layer 210 is a HDP oxide layer," column 3, line 35 and discloses "oxide spacer 210a," column 3, line 43. Thus, spacer 210a does not appear to be formed of silicon nitride.

Claim 18 includes the limitation, "the plane of the second floating gate portion bisects the first floating gate portion." This limitation does not appear to be shown by Chiu. In particular the cited portion of Chiu (Figures 1-2) appear to show second floating gate portions that extend along planes at either end of first floating gate portions. For example, Figure 2E shows patterned conductive layer 214a that contacts first conductive layer 202 along a surface and extends up from this surface at either end. However, both of the portions that extend up are near ends of first conductive layer 202 and neither would appear to be along a plane that bisects first conductive layer 202. Because this limitation is not shown, claim 18 is submitted to be allowable. Claim 18 is amended to clarify that the process is self-aligned.

Claim 19 depends from claim 18 and is submitted to be allowable for at least the reasons given with respect to claim 18. In addition claim 19 recites that the first floating gate portions are square in shape, which does not appear to be disclosed by Chiu. The limitation "the second portions extend from a line that is approximately a midline of the square" also does not appear to be disclosed by Chiu because, as discussed with respect to claim 18, Chiu appears to show any vertical extensions being from either end of first conductive layer 202. Thus, claim 19 is submitted to be additionally allowable over Chiu.

**Claim Rejections under 35 USC 103**

Claims 2-5 and 8-12 are rejected under 35 USC 102 as being unpatentable over Chiu in view of Chuang (US Pub. No. 2004/0033663). Claims 2-5 and 8-12 are submitted to be allowable at least for depending from claim 1, which is believed to be allowable as discussed above. In addition, certain of these claims have additional distinctions over the cited references.

Claim 3 recites "implanting impurities into the substrate while first floating gate portions covered by dielectric are present." The Office Action stated, "it is inherent that for devices in Chiu and Chuang et al., source/drain regions are required and source/drain regions are formed by implanting impurities and formed into the substrate besides the gate." However, this does not address the underlined portion of the above limitation. Implantation could be done at another time and alignment between source/drain regions and gates could be provided by separate alignment steps. The present application shows a self-aligned process that advantageously uses the gates as a mask layer for implantation of source/drain regions. Chiu and Chuang do not appear to show this limitation as part of their inventions, nor is this limitation believed to be inherent.

Claim 10 recites, "the conductive gates extend towards the surface of the semiconductor substrate such that the lowest extremities of the conductive gates are closer to the surface of the semiconductor substrate than the highest extremities of the second floating gate portions." Chuang was cited as showing this feature. However, no motivation to combine the references to obtain the combination of claim 10 is given. MPEP 2143.01 states, "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art suggests the desirability of the combination." Here, no such suggestion is provided. Therefore, claim 10 is believed to be additionally allowable.

Claim 11 recites, "The method of claim 10 wherein the conductive gates extend to enclose the second floating gate portions from above and on four lateral sides." This limitation does not appear to be shown by either of the cited references. Chuang was cited as showing this feature in Figure 2i. However, Figure 2i appears to show conductive gates extending along only one lateral side of conductive protruding layer 209a. It appears that there is one control gate 212 for a pair of conductive protruding layers 209a. Control gate 212 extends along only one lateral side of one conductive gate. Control gate 212 does not appear to extend down the opposing lateral side. In addition, there appears to be no indication as to whether control gate 212 encloses conductive protruding layers 209a in a plane perpendicular to the plane of the cross-section shown in Figure 2i. Thus, enclosure is clearly not present on one lateral side, and is not shown on two remaining sides. In addition, no motivation is provided for modifying Chiu to have

this feature of claim 11. Therefore, claim 11 is submitted to be additionally allowable over the cited references.

## CONCLUSION

In view of the amendments and remarks contained herein, it is believed that all claims are in condition for allowance and an indication of their allowance is requested. However, if the Examiner is aware of any additional matters that should be discussed, a call to the undersigned attorney at: (415) 318-1160 would be appreciated.

Respectfully submitted,

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